WHAT IS CLAIMED IS:

1   1.   A method for converting serial data to parallel data, the method

2 comprising:

3   serially loading bits of data into a first register in response to a first periodic

4 . signal;

5   parallel loading bytes of the data from the first register into a second register in

6 response to a second periodic signal; and

7   changing boundaries between the data bytes in response to a third signal.

1   2.   The method of claim 1 wherein changing the boundaries between the data

2 bytes in response to a the third signal further comprises changing the phase of the second

3 periodic signal in response to the third signal, wherein the change in the phase of the second

4 periodic signal causes one of the bits of the data stored in the first register to be discarded.

1   3.   The method of claim 1 further comprising:

2   parallel loading the data bytes from the second register into a third register.

1   4.   The method of claim 3 further comprising:

2   generating fourth and fifth periodic signals, wherein the third register

3 synchronizes the data bytes to the fourth periodic signal in response to the fifth periodic signal,

4 and wherein the fourth periodic signal is used as a clock signal by core circuitry that receives the

5 data from the third register.

1   5.   The method of claim 3 further comprising:

2   parallel loading the data bytes from the third register into core circuitry of a

3 . programmable logic device.

1   6.   The method of claim 1 further comprising:

2   generating the first periodic signal using a phase lock loop; and

3   providing the first periodic signal to an input of a first counter, wherein the first

4 counter generates the second periodic signal.

1   7.   The method of claim 6 further comprising:

2   parallel loading the data bytes from the second register into a third register; and

3   providing the first clock signal to an input of a second counter, wherein the

4   second counter generates a fourth periodic signal that controls when the data bytes are loaded

5   into the third register.

1   8.   The method of claim 1 further comprising:

2   disabling the third signal to prevent the boundaries between the data bytes from

3   changing.

1   9.   The method of claim 1 wherein changing the boundaries between the data

2   bytes in response to the third signal further comprises realigning a data boundary between bytes

3   of the data bytes by one bit in response to the second periodic signal.

1   10.   The method of claim 9 wherein changing the boundaries between the data

2   bytes in response to the third signal further comprises realigning a data boundary between bytes

3   of the data bytes by two bits in response to the second periodic signal.

1   11.   A serial-to-parallel data conversion circuit comprising:

2   a first register coupled to receive serial data;

3   a second register coupled to receive parallel data bytes from the first register; and

4   a first counter circuit providing a first periodic signal that controls when the

5   parallel data bytes are transferred from the first register to the second register, the first periodic

6   signal causing boundaries between the parallel data bytes to change in response to a second

7   signal.

1   12.   The serial-to-parallel data conversion circuit of claim 11 further

2   comprising:

3   a phase locked loop circuit that provides a third periodic signal to the first and

4   second registers and to the first counter, wherein data is shifted through the first and second

5   registers in response to the third periodic signal.

1   13.   The serial-to-parallel data conversion circuit of claim 11 further

2   comprising:

3   a third register coupled to receive the parallel data bytes from the second register;

4   and

5   a second counter circuit providing a third periodic signal that controls when the

6   parallel data bytes are transferred from the second register into the third register.

1   14.   The serial-to-parallel data conversion circuit of claim 13 wherein the third

2   register synchronizes the parallel data to a fourth periodic signal generated by the second

3   counter.

1   15.   The serial-to-parallel data conversion circuit of claim 13 further

2   comprising:

3   a fourth register coupled between the first counter and the second register; and

4   a fifth register coupled between the second counter and the third register.

1   16.   The serial-to-parallel data conversion circuit of claim 11 further

2   comprising:

3   a third register coupled to the first counter, the third register generating the second

4   signal, wherein an input of the third register is coupled to receive a fourth signal that blocks the

5   second signal.

1   17.   A method for converting serial data to parallel data, the method

2   comprising:

3   loading bits of the serial data into a first data storage circuit in response to a first

4   periodic signal;

5   loading the bits from the first data storage circuit into a second data storage circuit

6   as parallel data bytes in response to a second periodic signal, wherein boundaries between the

7   parallel data bytes are determined by the second periodic signal; and

8   shifting the boundaries between the parallel data bytes in response to a third

9   signal.

1   18.   The method of claim 17 wherein shifting the boundaries between the

2   parallel data bytes in response to the third signal further comprises increasing the period of the

3   second periodic signal in response to the third signal.

1   19.   The method of claim 17 further comprising:

2   loading the parallel data bytes from the second data storage circuit into a third

3 data storage circuit; and

4   generating a fourth periodic signal that controls when the data bytes are loaded

5 · into the third data storage circuit.

1   20.   The method of claim 17 further comprising:

2   generating the first periodic signal using a phase lock loop; and

3   providing the first periodic signal to an input of a first counter, wherein the first

4 counter generates the second periodic signal.

1   21.   The method of claim 17 further comprising:

2   disabling the third signal to prevent the boundary between parallel data bytes from

3 shifting.

1   22.   A serial-to-parallel data converter comprising:

2   means for storing bits of serial data in a first storage circuit;

3   means for storing the bits as parallel data bytes in a second storage circuit;

4   means for providing a first periodic signal that controls when the bits are

5 transferred from the first storage circuit to the second storage circuit; and

6   means for providing a second signal to the means for providing the first periodic

7 signal, wherein the first periodic signal causes a boundary between the parallel data bytes to

8 change by at least one bit in response to the second signal.

1   23.   The serial-to-parallel converter of claim 22 further comprising:

2   means for storing the parallel data bytes in a third storage circuit; and

3   means for providing a third periodic signal that controls when the parallel data

4 bytes are transferred from the second storage circuit to the third storage circuit.

1   24.   The serial-to-parallel converter of claim 22 further comprising:

2   means for generating a third periodic signal using a phase locked loop, wherein

3 the third periodic signal is provided to the first and the second storage circuits and to the means

4 for providing the first periodic signal.